

What Is Claimed Is:

- 1 1. Apparatus for managing flow of information among plural
2 processors of a processing array, comprising:
3 a system bus for interconnecting at least two processors; and
4 means for arbitrating access to at least a first portion of a system bus
5 among said at least two processors to transfer information over said first
6 portion, said information being transferred using a protocol by which a system
7 bus performs control actions for system bus access independently of said at least
8 two processors.
- 1 2. The apparatus of claim 1, comprising:
2 at least one module connected by said system bus to said means for
3 arbitrating.
- 1 3. The apparatus of claim 2, wherein said at least one module
2 comprises a gateway device for communicating via said system bus to said
3 means for arbitration.
- 1 4. The apparatus of claim 3, wherein said at least one module
2 comprises a module bus for administering to at least one module node within
3 said at least one module.
- 1 5. The apparatus of claim 4, wherein said at least one module node
2 comprises a processing device.
- 1 6. The apparatus of claim 5, wherein said at least one module node
2 comprises a bus interface device for achieving data communication between said
3 processing device and said module bus.

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1 7. The apparatus of claim 6, wherein said at least one module
2 comprises a local processor bus for communicating data between said processing
3 device and said bus interface device.

1 8. The apparatus of claim 1, comprising:
2 a sensor interface connected to said system bus.

1 9. The apparatus of claim 8, wherein said sensor interface
2 comprises a processor for processing sensor data.

1 10. The apparatus of claim 9, wherein said sensor interface
2 comprises a bus interface device for communicating data between said processor
3 and said system bus.

1 11. The apparatus of claim 10, wherein said sensor interface
2 comprises a local processor bus for communicating data between said processor
3 and said bus interface device.

1 12. The apparatus of claim 8, wherein said sensor interface
2 comprises a video sensor interface.

1 13. The apparatus of claim 8, wherein said sensor interface
2 comprises a forward looking infrared (FLIR) sensor interface.

1 14. The apparatus of claim 1, comprising a system controller for
2 controlling access to the system bus.

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1 15. The apparatus of claim 14, wherein said system controller
2 comprises a system bus arbitration unit for controlling access to the system bus.

1 16. The apparatus of claim 14, wherein said system controller
2 comprises a processor connected to a bus interface device, which is connected to
3 the system bus.

1 17. A method for managing the flow of information among plural
2 processors of a processing array, comprising the steps of:
3 interconnecting at least two processors by a system bus; and
4 arbitrating access to at least a first portion of a system bus among said at
5 least two processors to transfer information over said first portion, said
6 information being transferred using a protocol by which a system bus performs
7 control actions for system bus access independently of said at least two
8 processors.

1 18. The method of claim 17, comprising the step of:
2 interconnecting at least one module with said system bus by way of a bus
3 gateway device, said at least one module comprising said bus gateway device, a
4 module bus, at least one processor, and at least one bus interface device for
5 connecting said at least one processor to said module bus.

1 19. The method of claim 18, wherein said step of arbitrating
2 comprises the steps of:
3 establishing a clear path to a device by checking device busy signals to
4 ensure that a destination device is not busy;
5 requesting a bus grant to transmit data packets to said device;

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24. The method of step 23, wherein the system bus arbitration unit grants access to a second device upon request during a transmission of a data packet by another device on the system bus.

1 25. The method of claim 24, wherein access to the system bus is
2 granted to a second device by the system bus arbitration unit, which executes
3 the steps of:
4 discontinuing bus grant access to any device currently transmitting data;
5 verifying that the system bus is not busy;
6 verifying that a destination device is not busy;
7 granting access to the system bus for the second device requesting
8 access;
9 delaying any further transmission by said device whose access to the
10 system bus was discontinued by said step of discontinuing until after at least one
11 data packet has been transmitted by said second device.

1 26. The method of claim 25, wherein access to the system bus
2 between multiple devices connected to the system bus is granted according to
3 priority.

1 27. The method of claim 26, wherein access to the system bus
2 between multiple devices connected to the system bus is granted in a rotating
3 fashion based on said priority and for a maximum of the time required to
4 transfer one data packet.

1 28. The method of claim 17, wherein devices connected to the system
2 bus contain local and module busses connected to the system bus by way of a
3 gateway device, which arbitrates access to nodes connected to said module bus.

1 29. The method of claim 28, wherein said gateway device arbitrates
2 access to the local and module busses according to priority.

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1 30. The method of claim 29, wherein said gateway device arbitrates
2 access to the local and module busses in a rotating fashion.

1 31. The method of claim 28, wherein arbitration of access to the
2 module bus is accomplished by the following steps:
3 inquiring if the module bus is in use;
4 verifying that a destination processor is not busy once the module bus is
5 not in use;
6 requesting access to the module bus to a bus gateway device;
7 gaining access to the module bus from said bus gateway device; and
8 transmitting data packets to said destination device.

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